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TITLE

MONOTONIC LEAKAGE-TOLERANT LOGIC CIRCUITS

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BACKGROUND OF THE INVENTION

Field of the Invention

[001] The present invention relates in general to the field of logic circuits and, more specifically, to an improved logic methodology that combines the speed advantages of dynamic logic with the low contention of static logic, such that the circuits are not adversely affected by high leakage transistors. This is accomplished through the use of a circuit comprising leakage-tolerant dynamic and static logic.

Description of the Related Art

[002] As semiconductor fabrication processes continue to advance, the leakage current (i.e., the residual current through a transistor when it is supposed to be "off") continues to increase at an exponential rate. This leakage current causes unwanted power dissipation as well as functional problems for dynamic logic.

[003] In a dynamic logic circuit, there is a precharged node that must maintain its value near V_{dd} during the evaluation phase in order for the circuit to work properly. This is usually done by adding a small pMOS transistor (keeper) whose drain is connected to the precharge node, source is connected to V_{dd}, and gate is connected to the circuit output (i.e., the precharge node through an inverting static gate).

[004] With the very high leakage currents of modern process technologies, the keeper must be so large for most types of dynamic circuits that the speed of the

dynamic circuit is adversely affected, thus eliminating one of the primary reasons for using dynamic circuits. The speed is hindered because the dynamic logic nMOS pull-down evaluation transistors must "fight" (or "contend with") the keeper in order to switch the gate logic value.

[005] In view of the foregoing, there is a need for improved logic circuitry that has speed similar to dynamic logic, but with the leakage insensitivity of static logic.

SUMMARY OF THE INVENTION

[006] The method and apparatus of the present invention overcomes the shortcomings of the prior art by providing an improved logic methodology that combines the speed advantages of dynamic logic with the low contention of static logic, such that the circuits are not adversely affected by high leakage transistors. In the present invention, this is accomplished through the use of a circuit comprising leakage-tolerant dynamic and static logic.

[007] In one embodiment of the present invention, the first logic stage of a logic circuit comprises clocked precharge and evaluate transistors and full-complementary low-beta-ratio static logic. Subsequent stages of the logic comprise full-complementary low-beta-ratio static logic, wherein the logic devices in said subsequent stage are not connected to a clock signal. The low-beta-ratio static logic in said subsequent stage does not use a contention keeper. Furthermore, in the present invention, the low-beta-ratio static logic transistors in the subsequent stage comprise pMOS transistors that are significantly smaller than pMOS devices found in normal static logic.

[008] The first stage of the logic circuit of the present invention comprises a tapered nMOS stack having a clocked nMOS transistor at the top of the stack and further comprises static pMOS pull-up transistors in place of a traditional contention keeper. Subsequent stages of the logic circuit of the present invention comprise tapered nMOS stacks without clock transistors and small pMOS pull-up devices. The pMOS devices have sizes that are based on predetermined criteria to maximize performance and minimize surface area. The minimum effective pMOS width is selected as the minimum width that will provide sufficient precharge for the gate. This effective width can be distributed across all of the pull-up pMOS transistors in the stage. Each pMOS transistor has a size that is only large enough to be effective for counteracting current leakage.

BRIEF DESCRIPTION OF THE DRAWINGS

[009] The present invention may be better understood, and its numerous objects, features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference number throughout the several figures designates a like or similar element.

[010] Figure 1 is an illustration of the first and second phases of a conventional dynamic logic circuit.

[011] Figure 2 is an illustration of the first and second phases of a conventional logic circuit having a tapered transistor stack in the first stage.

[012] Figure 3 is an illustration of the first and second phases of the monotonic leakage-tolerant logic circuit of the present invention.

DETAILED DESCRIPTION

[013] Figure 1 is an illustration of a conventional dynamic logic circuit 100 comprising a first stage 101 and second stage 101a. The dynamic logic circuit 100 comprises input nMOS transistors 102, 104, and 106 that receive logic input signals "A," "B," and "C," respectively. During the precharge phase, the clock signal CLK is LOW and, therefore, the nMOS transistor 112 is OFF and the pMOS transistor 110 is ON, thereby pulling node 108 HIGH. During the evaluation phase, the clock signal CLK is HIGH and, therefore, the pMOS transistor 110 is turned OFF and the nMOS transistor 112 is turned ON. During the evaluation phase, the nMOS transistors 102, 104, and 106 conditionally pull node 108 LOW, depending on the values of the input signals A, B, and C. A keeper comprising inverter 114 and pMOS transistor 116 maintains node 108 HIGH unless it is otherwise pulled LOW by the nMOS transistors 102, 104, and 106 during the evaluation phase. The output of the inverter 114 is provided to additional stages of the logic circuit, such as the second stage illustrated in Figure 1. The components in the second stage of the phase illustrated in Figure 1 are substantially identical to the corresponding components discussed in connection with the first stage and, therefore, their function will not be repeated.

[014] The effect of the keeper in the prior art circuit 100 of Figure 1 can be understood by referring again to the first stage 101. Since node 108 is initially HIGH, the output of the inverter 114 is initially LOW. The output of the inverter 114 will transition from LOW to HIGH during the evaluation phase only if the inputs A, B, and C are all HIGH. For the input signal condition where the output of the inverter 114 remains LOW (i.e., A, B, or C is LOW), there is no transition of the output signal and, therefore, the operational speed of the dynamic logic circuit is not adversely

affected. For the input signal condition where the output of the inverter 114 transitions from LOW to HIGH, however, the ability of the inverter 114 to transition quickly and accurately can affect the operational speed of the dynamic logic circuit. In summary, there is a need to optimize the design of the logic stage for "pull-down" and to optimize the inverter 114 for "pull-up."

[015] As was discussed hereinabove, the dynamic logic circuit 100 illustrated in Figure 1 requires a relatively strong contention keeper because of the high leakage currents of transistors fabricated using current process technologies. A strong contention keeper, however, can adversely affect the speed of the circuit. Specifically, the speed of the dynamic logic circuit 100 is hindered because the nMOS pull-down evaluation transistors 102, 104, and 106 must "fight" the keeper in order to switch the gate logic value. The compromised speed seriously diminishes the value of the dynamic logic circuit 100 illustrated in Figure 1 for many applications.

[016] The widths of the various transistors used in the traditional dynamic logic circuit illustrated in Figure 1 are denoted by the reference numerals adjacent to each transistor. For example, the input nMOS transistors 102, 104, 106 and the nMOS transistor 112 each have a width of 10 microns. The pMOS transistor 110 illustrated in Figure 1 has a width of 3 microns, while the pMOS device 116 used in the keeper has a width of 0.5 microns. The dimensions of the corresponding circuit components in the second stage of the phase have the same dimensions as those discussed in connection with the first phase of the dynamic logic circuit 100. Similar reference numerals will be used to denote the size of transistors of the dynamic logic circuits illustrated in Figures 2 and 3. The size of the various circuit components will be discussed for purposes of illustrating the operating characteristics and advantages

of the present invention. As will be understood by those of skill in the art, however, other dimensions can be used for the various circuit components, depending on the specific fabrication process, without departing from the teachings of the present invention.

[017] Figure 2 is an illustration of another prior art logic circuit 200 comprising a first stage 202 having a tapered stack of input transistors and a second stage 201a wherein the stack of input transistors is not tapered. As can be seen in Figure 2, data inputs A, B, and C for the first stage are received by nMOS transistors 202, 204, and 206, respectively. The clock signal CLK for the first stage is provided as an input to the gates of pMOS transistor 208 and nMOS transistor 210. When the clock signal CLK is LOW, the nMOS transistor 210 will be turned OFF and the pMOS transistor 208 will be turned ON, thereby maintaining node 205 HIGH at a voltage approximately equal to V_{dd}. During the evaluate phase, the clock signal CLK will go HIGH, thereby turning pMOS transistor 208 OFF and turning nMOS transistor 210 ON.

[018] As can be seen in Figure 2, the gates of the respective input nMOS transistors in the first stage 201 are tied to the gates of the corresponding pMOS pull-up transistors. For example, the gate of nMOS transistor 202 is tied to the gate of pMOS transistor 214. Likewise, the gate of input transistors 204 and 206 are tied to the gates of pMOS pull-up transistors 216 and 218, respectively.

[019] The second stage 201a of the prior art logic circuit 200 illustrated in Figure 2 comprises a static logic circuit that does not receive a clock signal input. The gates of the respective input nMOS transistors in the second stage 201a are tied to the gates of the corresponding pMOS pull-up transistors. For example, the gate of

nMOS transistor 202a is tied to the gate of pMOS transistor 220. Likewise, the gates of input transistors 204a and 206a are tied to the gates of pMOS pull-up transistors 222 and 224, respectively.

[020] The stack of nMOS transistors in the first stage of the logic circuit 200 are "tapered" to improve performance by compensating for the performance effects related to the capacitances created by various nMOS transistors in the stack. For example, the nMOS transistors 210, 202, 204, and 206 have widths of 5 microns, 7 microns, 8 microns, and 10 microns, respectively. The stack of nMOS transistors in the second stage of the circuit 200, however, is not tapered. Each of the nMOS transistors 202a, 204a, and 206a have widths of 9 microns. Furthermore, each of the pMOS pull-up transistors 220, 222, and 224 have widths of 3 microns.

[021] Figure 3 is an illustration of the monotonic leak-tolerant circuit 300 of the present invention comprising both leakage-tolerant clocked logic and static logic. In the embodiment illustrated in Figure 3, the present invention comprises a first stage of logic that has both clocked precharge and evaluate transistors as well as full-complementary low-beta-ratio static logic. In the improved logic circuit 300 of the present invention, both the first and second stages of the circuit comprise tapered stacks of nMOS input transistors. In addition, the subsequent stage of logic illustrated in Figure 3 comprises full-complementary low-beta-ratio static logic. However, the subsequent stage does not comprise clock inputs.

[022] The use of low-beta-ratio static logic in the second stage of the logic circuit 300 is a significant aspect of the present invention. In the context of the present invention, "low-beta-ratio" logic comprises pMOS transistors that are significantly smaller than would be used in conventional static logic. This saves

surface area on the integrated circuit and also improves the speed of the circuit pull-down by reducing the cross-over contention between the nMOS and pMOS transistors during the transition.

[023] As can be seen in Figure 3, data inputs A, B, and C for the first stage are received by nMOS transistors 302, 304, and 306, respectively. The clock input for the first stage is provided as an input to the gates of pMOS transistor 308 and nMOS transistor 310. When the clock is LOW, pMOS transistor 308 will be turned ON, thereby maintaining node 305 HIGH at a voltage approximately equal to V_{dd}. During the evaluate phase, the clock signal CLK will go HIGH, thereby turning nMOS transistor 310 ON.

[024] The first stage of the logic circuit illustrated in Figure 3 comprises a tapered nMOS stack of transistors 302, 304, and 306 with a clocked nMOS transistor 310 at the top of the stack. As discussed above in connection with the prior art tapered logic circuit 200, the first stage of the phase further comprises static pMOS pull-up transistors rather than a contention keeper. In the logic circuit 300 of the present invention, however, subsequent stages of the phase also comprise a tapered stack of nMOS input transistors but without a clocked transistor in the stack.

[025] As can be seen in Figure 3, the gates of the respective nMOS input transistors in the first stage 301 are tied to the gates of the corresponding pMOS pull-up transistors. For example, the gate of nMOS transistor 302 is tied to the gate of pMOS transistor 314. Likewise, the gate of input transistors 304 and 306 are tied to the gates of pMOS pull-up transistors 316 and 318, respectively.

[026] The second stage 301a of the phase of the logic circuit 300 comprises a static logic circuit that does not receive a clock signal input. The gates of the

respective input nMOS transistors are tied to the gates of the corresponding pMOS pull-up transistors. For example, the gate of nMOS transistor 302a is tied to the gate of pMOS transistor 320. Likewise, the gate of input transistors 304a and 306a are tied to the gates of pMOS pull-up transistors 322 and 324, respectively.

[027] The stack of nMOS transistors in both the first stage and the second stage of the logic circuit 300 are "tapered" to improve performance by compensating for the performance effects related to the capacitances created by various nMOS transistors in the stack. For example, the nMOS transistors 210, 202, 204, and 206 have widths of 5 microns, 7 microns, 8 microns, and 10 microns, respectively, as discussed above in connection with the prior art logic circuit 200. The stack of nMOS transistors in the second stage of the improved logic circuit 300, however, is also tapered. The nMOS input transistors 302a, 304a and 306a have widths of 5 microns, 7 microns and 9 microns, respectively.

[028] The small pMOS pull-up transistors are sized based on design criteria that ensure efficient performance and acceptable leakage tolerance. Each of the pMOS pull-up transistors 314a, 316a, and 318a have widths of 0.5 microns, although those of skill in the art will recognize that other widths for these transistors can be implemented without departing from the teachings of the present invention. As will be understood by those of skill in the art, the ratio of dimensions of the pMOS transistors and the respective nMOS transistors in the tapered stack resulting in a beta-ratio that is substantially less than 1:1. The minimum effective pMOS width only needs to be enough to "precharge" the gate. This effective width can be distributed across all the pMOS transistors 314a, 316a, and 318a. Furthermore, the minimum size for each PMOS transistor needs to only be enough to combat leakage.

[029] The present invention offers numerous advantages over prior art logic circuits and is able to overcome the functional problems associated with transistors fabricated using current process technologies. The logic circuit of the present invention combats current leakage without the use of contention keepers, thereby offering improved performance in terms of speed. In addition, the logic circuit of the present invention provides lower clock loading than traditional dynamic logic circuits due to the tapering of the transistor stacks in the subsequent stages and because the subsequent stages do not require a clock signal. Furthermore, the logic circuit of the present invention requires less area in the integrated circuit due to the reduced size of the pMOS transistors used in place of traditional contention keepers. Finally, the logic circuit of the present invention has a very low skew because the precharge is distributed across multiple pMOS devices.

Other Embodiments

Other embodiments are within the following claims. The invention disclosed herein is susceptible to various modifications and alternative forms. Specific embodiments therefore have been shown by way of example in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims.